WHAT IS CLAIMED IS:

1. An SRAM device, comprising:

an SRAM array coupled to an SRAM array low voltage source that provides a low SRAM array supply voltage V_{SB} to said SRAM device; and

main column peripheral circuitry having main pre-charge circuitry free of an SRAM header, coupled to said SRAM array by bit lines and coupled to a sleep mode controller through an associated main column peripheral driving circuitry that is configured to isolate said bit lines from a power supply during a sleep mode.

2. The SRAM device as recited in Claim 1 wherein said main column peripheral circuitry further includes a main column MUX, main write circuitry and a main sense amp.

3. The SRAM device as recited in Claim 2 wherein said sleep mode controller is configured to isolate said bit lines by employing said main column peripheral driving circuitry to turn off circuitry selected from the group consisting of:

said main pre-charge circuitry,

said main column MUX,

said main write circuitry, and

said main sense amp.

4. The SRAM device as recited in Claim 1 wherein said main column peripheral driving circuitry includes circuitry selected from the group consisting of:

main pre-charge driving circuitry,

main write driving circuitry,

main column MUX driving circuitry, and

main sense amp driving circuitry.

5. The SRAM device as recited in Claim 1 wherein an output of said main column peripheral driving circuitry is clamped at an array reference voltage V_{BB} during said sleep mode.

6. The SRAM device as recited in Claim 1 wherein said main column peripheral circuitry further includes a main sense amp free of an SRAM header.

7. The SRAM device as recited in Claim 1 wherein said SRAM array low voltage source is a sinking low drop-out voltage regulator.

8. The SRAM device as recited in Claim 1 wherein said sleep mode controller is a pMOSFET.

9. The SRAM device as recited in Claim 1 wherein said SRAM array low voltage source raises said low SRAM array supply voltage V_{SB} to an array reference voltage V_{BB} during sleep mode.

10. The SRAM device as recited in Claim 1 wherein said sleep mode controller is configured to isolate said bit lines from a high power supply.

11. The SRAM device as recited in Claim 1 wherein an output voltage of said main pre-charge driving circuitry is raised during sleep mode to turn off said main pre-charge circuitry.

12. The SRAM device as recited in Claim 11 wherein said output voltage is raised to about said low SRAM array supply voltage V_{SB}.

13. The SRAM device as recited in Claim 1 wherein said sleep mode controller includes a row header.

14. A method of powering-down an SRAM device having main column peripheral circuitry coupled to an SRAM array by bit lines, comprising:

transmitting a power down signal to an SRAM array low voltage source coupled to said SRAM array that raises a low SRAM array supply voltage V_{SB} to an SRAM array reference voltage V_{BB}; and

providing said SRAM array reference voltage V_{BB} to a sleep mode controller, coupled to said main column peripheral circuitry by a main column peripheral driving circuitry, to isolate said bit lines from a power supply.

15. The method as recited in Claim 14 wherein said main column peripheral circuitry includes main pre-charge circuitry, a main column MUX, main write circuitry and a main sense amp.

16. The method as recited in Claim 15 wherein said sleep mode controller isolates said bit lines by employing said main column peripheral driving circuitry to turn off circuitry selected from the group consisting of:

said main pre-charge circuitry,

said main column MUX,

said main write circuitry, and

said main sense amp.

17. The method as recited in Claim 14 wherein said main column peripheral driving circuitry includes circuitry selected from the group consisting of:

main pre-charge driving circuitry,

main write driving circuitry,

main column MUX driving circuitry, and

main sense amp driving circuitry.

18. The method as recited in Claim 14 further comprising clamping an output of said main column peripheral driving circuitry at an array reference voltage V_{BB}.

19. The method as recited in Claim 14 wherein said main column peripheral circuitry includes main pre-charge circuitry free of an SRAM header.

20. The method as recited in Claim 14 wherein said main column peripheral circuitry includes a main sense amp free of an SRAM header.

21. The method as recited in Claim 14 wherein said SRAM array low voltage source is a sinking low drop out voltage regulator.

22. The method as recited in Claim 14 wherein said sleep mode controller is a pMOSFET.

23. The method as recited in Claim 14 wherein said sleep mode controller isolates said bit lines from a high power supply.